Claims

Amend claims 2-5 and add claims 8-12 follows:

1.(Currently Amended) A circuit arrangement for transferring data between a data transmitter and a plurality of data receivers, said circuit arrangement comprising:

a buffer device that receives a data signal from the data transmitter and provides a buffered data signal onto a data bus;

a first memory element configured and arranged a non-sequential component coupled to said data bus to ~~that~~ receives and stores said buffered signal ~~on said data bus~~ and provides a first stored signal;

a plurality of second memory elements ~~that~~ receives and stores said first stored signal and each provides an associated second stored signal to its associated one of said plurality of ~~the~~ data receivers; and

a controller that controls the output state of said buffer device, to control the transfer of data from said first memory element to said second memory element.

2.(Currently Amended) The circuit arrangement of claim 1, wherein said first memory element comprises ~~by inherent~~ parasitic capacitance associated with said data bus.

3.(Currently Amended) The circuit arrangement of claim 1, wherein said first memory device comprises ~~is constructed as~~ a capacitive element, one of whose terminals is connected to said data bus, and whose other terminal is connected to a reference potential.

4.(Original) The circuit arrangement of claim 3, wherein capacitance of said capacitive element is

provided by the line capacitance of said data bus with respect to one or more reference lines.

5.(Currently Amended) The circuit arrangement of claim 2, wherein said first memory element~~device~~ comprises a dedicated memory element that comprises a holding element.

6.(Currently Amended) The circuit arrangement of claim 3, wherein said controller controls said data buffers ~~(P1, P2)~~ associated with the data transmitter ~~(S)~~ and the data receivers ~~(E)~~, and the second memory devices ~~(Sp2)~~.

7.(Currently Amended) The circuit arrangement of claim 1, wherein said controller comprises:

a first control section, associated with the data transmitter, for controlling the first data buffer; and

a second control section, associated with each of the data receivers, that controls second data buffers and said second memory devices, ~~a~~ to control data communication between the data transmitter and the data receiver.

8.(Currently Amended) The circuit arrangement of claim 7, wherein at least one of the circuit sections ~~(1, 2)~~ is part of a peripheral region ~~(2)~~ of the integrated circuit for accepting the connection pads of the input/output connections.

9.(Currently Amended) The circuit arrangement of claim 1, wherein the circuit arrangement has at least one microprocessor/microcontroller and/or at least one signal processor ~~with a given set of states~~.

10.(Original) The circuit arrangement of claim 1, wherein said first memory element consists of parasitic capacitance associated with said data bus.

11.(Currently Amended) An integrated circuit arrangement for transferring data between a data transmitter and a plurality of data receivers, said circuit arrangement comprising:

means for receiving a data signal from the data transmitter and for providing a buffered data signal onto a data bus;

a first non-sequential memory element coupled to said data bus to ~~that~~ receives and stores said buffered data signal ~~on said data bus~~, and provides a first stored signal;

a plurality of second memory elements that each receives and stores said first stored signal, and provides a second stored signal to its associated one of the plurality of ~~the~~ data receivers; and

a controller that selectively enables the storage of said buffered data signal in said first memory element and the storage of said first stored signal in said plurality of second memory elements.

~~a controller that controls the output state of said means for receiving, such that when said means for receiving provides a high impedance output data is transferred from said first memory element to said second memory element.~~

12.(New) The circuit arrangement of claim 11, wherein said first memory element consists of parasitic capacitance associated with said data bus.

13.(New) The circuit arrangement of claim 11, wherein said first memory element comprises a

capacitive element having a first lead and a second lead, wherein said first lead connected to said data bus, and said second lead is connected to a reference potential.

14.(New) The circuit arrangement of claim 11, wherein said first memory element is provided by the line capacitance of said data bus with respect to one or more reference lines.

15.(New) An integrated circuit arrangement for transferring data between a data transmitter and a plurality of data receivers also located on the integrated circuit arrangement, said circuit arrangement comprising:

a receiving circuit for receiving a data signal from the data transmitter and for providing a buffered data signal onto a data bus;

a capacitive element coupled to said data bus to receive and store said buffered data signal, and provide a first stored signal;

a plurality of memory elements that receive and store said first stored signal, and provides a second stored signal to an associated one of said plurality of data receivers; and

a controller that selectively enables the transfer of information into said capacitive element and said memory elements.